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In the claims:

1.-3.   (cancelled)

4.   (currently amended) A multiprocessor computer system capable of being partitioned into
one or more independently functioning processing systems comprising:

        a plurality of processing nodes, each node including memory which is accessible locally by
the node associated with said memory and remotely by any other node;

        a shared, distributed system memory;

        a communications pathway which interconnects said plurality of processing nodes, each
node capable of operating independently, wherein each one of said processing nodes includes at
least one processor and a portion of said shared system memory coupled to said processor and
said communication pathway, and wherein said communication pathway is comprised of a central
hardware device including tag and address means to communicate the identification of data
transactions being processed through the system connected to said plurality of processing nodes,
said tag and address means including means to store information related to the identification of a
partition to which said data is associated, said central hardware device storing information for
determining which nodes are storing copies of data which is associated with a given partition;

        means to define one or more partitions to which one or more of said nodes are a member;
and

        means to associate each data transaction processed in the system to direct data only to
such nodes defined as within the same partition of said data, including dispatch means which
interconnect with said ports but allow communications with said ports only for data transactions
defined for a partition for which said port is a member.

5.-7.   (cancelled)

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8.   (currently amended) A multiprocessor computer system capable of being partitioned into one or more independently functioning processing systems comprising:

     a plurality of processing nodes, each node capable of operating independently;

     a shared, distributed system memory;

     a communications pathway which interconnects said plurality of processing nodes, wherein each one of said processing nodes includes at least one processor and a portion of said shared system memory coupled to said processor and said communication pathway, wherein said communication pathway is comprised of a central hardware device including tag and address means to communicate the identification of data transactions being processed through the system connected to said plurality of processing nodes, said tag and address means including a first register means to store information related to the identification of a partition to which said data is associated, and a second register means to define at most one partition to which one or more of said nodes are a member; and

     means to associate each data transaction processed in the system such as to direct data only to such nodes defined as within the same partition of said data,

     wherein said tag and address means further includes a registers means associated with each node, said register means separately connected through said communications pathway only to one of said nodes, whereby each of said register means is connected to only one of said nodes, wherein each said register means accepts and forwards data transactions only identified as valid for the partition which said register is connected.

9.   (cancelled)

10.   (currently amended) A multiprocessor computer system capable of being partitioned into one or more independently functioning processing systems comprising:

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        a plurality of processing nodes, each node capable of operating independently;

        a shared, distributed system memory;

        a communications pathway which interconnects said plurality of processing nodes, wherein each one of said processing nodes includes at least one processor and a portion of said shared system memory coupled to said processor and said communication pathway, wherein said communication pathway is comprised of a central hardware device including tag and address means to communicate the identification of data transactions being processed through the system connected to said plurality of processing nodes, said tag and address means including a first register means to store information related to the identification of a partition to which said data is associated, and a second register means to define at most one partition to which one or more of said nodes are a member; and

        means to associate each data transaction processed in the system such as to direct data only to such nodes defined as within the same partition of said data, ~~The system of claim 8~~ wherein ~~further~~ said tag and address means includes dispatch means which restrict output of data transactions to only nodes which are defined within the partition with which the data is identified, and a second target node which is the destination of the requested data, wherein further said central hardware device transmits requests from the said requesting node to the said target node but not to any other node.

11.   (currently amended) In a multiprocessor computer system comprising a plurality of processing nodes; a shared, distributed system memory; and a communication pathway connecting said processing nodes; wherein each one of said processing nodes includes at least one processor; and a portion of said shared system memory coupled to said processor and said communication pathway; each node including memory which is accessible locally by the node associated with said memory and remotely by any other node; said communications pathway comprised of communications ports each dedicated to communicating with one of said processing nodes; a

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method for partitioning the resources of the system into two or more partitions; the method
comprising the steps of:

      assigning a physical address to at least two of said ports;

      assigning a logical address to each said physical address;

      storing said logical address in a memory;

      defining each of said processing nodes to correspond to no more than one partition, such
that said ports are interconnected with a dispatch mechanism that allows communications with
said ports only for data transactions defined for a partition for which said port is a member, and;

      routing data within the system to correspond with the addresses of the resources defined
as a partition, via a central hardware device of said communication pathway storing information
for determining which nodes are storing copies of data which is associated with a given partition.

12.   (original) The method of claim 11 wherein one or more of said processing nodes may be
defined as corresponding to no partition.

13.   (original) The method of claim 11 further including the step of labeling data requests
within the system to a logical address corresponding to the partition issuing said request.

14.   (currently amended) In a multiprocessor computer system comprising a plurality of
processing nodes; a shared, distributed system memory; and a communication pathway connecting
said processing nodes; wherein each one of said processing nodes includes at least one processor;
and a portion of said shared system memory coupled to said processor and said communication
pathway; each node including memory which is accessible locally by the node associated with said
memory and remotely by any other node: said communications pathway comprised of
communications ports each dedicated to communicating with one of said processing rtes; a

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method for partitioning the resources of the system into two or more partitions; the method
comprising the steps of:

    assigning a physical address to each of said ports;

    assigning a logical address to each said physical address;

    storing said logical address in a memory;

    defining each logical address to correspond to no more than one partition, such that said
ports are interconnected with a dispatch mechanism that allows communications with said ports
only for data transactions defined for a partition for which said port is a member;

    assigning identification to each data transaction within the system which corresponds to
the logical address to which the transaction is associated;

    comparing said identified transaction with said logical address in memory corresponding
to only one partition; and

    routing data within the system to said ports defined as a member of the partition with
which the data is associated, via a central hardware device of said communication pathway storing
information for determining which nodes are storing copies of data which is associated with a
given partition.

15.   (original) The method of claim 14 further including the step of routing data requests
within the system to a cache memory within said communications pathway with a logical address
corresponding to the partition issuing said request, with said cache memory physically
interconnected only with a port assigned to a physical address.

16.   (currently amended) A multiprocessor computer system capable of being partitioned into
one or more independently functioning processing systems comprising:

    a plurality of processing nodes, each node capable of operating independently;

    a shared, distributed system memory;

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a communications pathway which interconnects said plurality of processing nodes,

wherein each one of said processing nodes includes at least one processor and a portion of said

shared system memory coupled to said processor and said communication pathway, wherein said

communication pathway is comprised of a central hardware device including a tag and address

mechanism to communicate the identification of data transactions being processed through the

system connected to said plurality of processing nodes, said tag and address mechanism including

a first register to store information related to the identification of a partition to which said data is

associated, and a second register to define at most one partition to which one or more of said

nodes are a member; and

a mechanism to associate each data transaction processed in the system such as to direct

data only to such nodes defined as within the same partition of said data,

wherein said tag and address mechanism further includes a registers associated with each

node, said register separately connected through said communications pathway only to one of said

nodes, whereby each of said register is connected to only one of said nodes, wherein each said

register accepts and forwards data transactions only identified as valid for the partition which said

register is connected.

17.   (cancelled)

18.   (currently amended) A multiprocessor computer system capable of being partitioned into

one or more independently functioning processing systems comprising:

a plurality of processing nodes, each node capable of operating independently;

a shared, distributed system memory;

a communications pathway which interconnects said plurality of processing nodes,

wherein each one of said processing nodes includes at least one processor and a portion of said

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shared system memory coupled to said processor and said communication pathway, wherein said

communication pathway is comprised of a central hardware device including a tag and address

mechanism to communicate the identification of data transactions being processed through the

system connected to said plurality of processing nodes, said tag and address mechanism including

a first register to store information related to the identification of a partition to which said data is

associated, and a second register to define at most one partition to which one or more of said

nodes are a member; and

            a mechanism to associate each data transaction processed in the system such as to direct

data only to such nodes defined as within the same partition of said data, ~~The system of claim 16~~

            wherein further said tag and address mechanism includes a dispatch mechanism which

restrict output of data transactions to only nodes which are defined within the partition with which

the data is identified, and a second target node which is the destination of the requested data,

wherein further said central hardware device transmits requests from the said requesting node to

the said target node but not to any other node.

19.   (added) The multiprocessor system of claim 4, wherein said tag and address means

further includes a register means associated with each node, said register means separably

connected through said communications pathway only to one of said nodes, whereby each of said

register means is connected to only one of said nodes, where each said register means accepts and

forwards data transactions only identified as valid for the partition which said register is

connected.

20.   (added) The multiprocessor system of claim 19, wherein further said tag and address

means includes dispatch means which restrict output of data transactions to only nodes which are

defined within the partition with which the data is identified, and a second target node which is the

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destination of the requested data, wherein further said central hardware device transmits requests from the said requesting node to the said target node but not to any other node.

21.   (added) The multiprocessor system of claim 8, wherein further said tag and address means includes dispatch means which restrict output of data transactions to only nodes which are defined within the partition with which the data is identified, and a second target node which is the destination of the requested data, wherein further said central hardware device transmits requests from the said requesting node to the said target node but not to any other node.

22.   (added) The multiprocessor system of claim 10, wherein further said tag and address means includes dispatch means which restrict output of data transactions to only nodes which are defined within the partition with which the data is identified, and a second target node which is the destination of the requested data, wherein further said central hardware device transmits requests from the said requesting node to the said target node but not to any other node.